REMARKS

Claims 1-10 and 28-36 are pending in this application. Claims 1, 5 and 33 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

Claims 1-10 and 28-36 stand rejected under 35 U.S.C. §102(b) as being anticipated by, or in the alternative, under 35 U.S.C. §103(a) as being obvious over the newly cited prior art reference, Yamamoto (JP-A 10-092865) for reasons stated on page 3 of the final Office action (Paper No. 14) dated on May 21, 2002. Specifically, in support of the rejection of independent claims 1, 5 and 33, the Examiner simply makes a blanket assertion that Yamamoto '865 discloses,

> "a semiconductor device (see entire disclosure) comprising an electrode pad (13), a stress cushioning layer 917), a lead wire (14), external electrodes (11), and a conductor protective layer (10) (see FIGs. 1-2)."

No other reasons or statements were provided in either the final Office Action (Paper No. 14) dated on May 21, 2002, or the Advisory Action (Paper No. 17) dated on October 8, 2002, to explain how Yamamoto '865 discloses or suggests all the novel features, including the feature "wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have [or include] means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line and exposing a range from said end face on said end

surface of said semiconductor elements to an inside of said cutting scribe line" as expressly defined in each of Applicants' base claims 1, 5 and 33.

Therefore, the rejection is respectfully traversed. Applicants submit that the features of the present invention are not disclosed under 35 U.S.C. §102(b) or suggested under 35 U.S.C. §103(a) by Yamamoto '865. As a result, Applicants respectfully request the Examiner to reconsider and withdraw these rejections for the following reasons.

First of all, the rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

Alternatively, the rule under 35 U.S.C. §103 is also well settled that obviousness that three basic criteria be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970).

In the present situation, the Examiner has ignored key limitations of Applicants' claims 1-10 and 28-36 when formulated a rejection under 35 U.S.C. §102(b). Likewise, the Examiner has ignored to treat the claim invention as a whole, failed to consider the same key limitations of Applicants' claims 1-10 and 28-36, and failed to provide any suggestion or motivation to modify Yamamoto '786 in order to arrive at Applicants' claims 1-10 and 28-36. Applicants will address the deficiencies of both the §102(b) rejection and §103(a) rejection *in seriatim* herein below:

As the only cited reference in support of both the §102(b) and §103(a) rejections, Yamamoto '865 only serves as background art of Applicants' disclosed invention. Specifically, on page 5, lines 5-12 of Applicants' original disclosure, Applicants cite Yamamoto '865 for disclosing:

> "a semiconductor device of a type in which a resin layer for cushioning stress is installed between external electrodes and semiconductor elements. Individual semiconductor devices are manufactured by processing units of semiconductor wafer in a batch and finally cutting each semiconductor wafer into pieces."

The problem of this type of semiconductor device as described by Yamamoto '865 is that,

> "a plurality of resin layers and external electrodes are formed in units of semiconductor wafers in a batch, and then each semiconductor wafer is cut (diced) into pieces, has a constitution such that the interfaces of a plurality of resin layers sequentially formed on each semiconductor wafer are exposed on the end face of each semiconductor package, so that when a large mechanical stress is applied to the interfaces of the plurality of resin layers at the time of dicing of the semiconductor wafer, **or** when a large thermal stress is applied to the interfaces of the plurality of resin layers due to sudden temperature changes at the time of mounting of the semiconductor package, the stress is centralized to the interfaces between the semiconductor element exposed on the end face of the semiconductor package and the plurality of resin layers, so that one or more of the plurality of resin layers are peeled off and the semiconductor package may be damaged.
>
> As mentioned above, such a known semiconductor device cannot always exhibit high reliability, and it is difficult to obtain a high manufacturing yield rate." See pages 5-6 of Applicants' original disclosure.

Because of the problems associated with Yamamoto '865, Applicants propose a semiconductor device in which a semiconductor element has at least a stress cushioning layer and a semiconductor protective layer, and **end faces of these layers are positioned inside the cutting scribe lines formed on a semiconductor wafer**, and **the range of the surface at the end of the semiconductor element from the end face to the inside of the scribe line is exposed**, see page 1, lines 5-15 of Applicants' original disclosure.

This arrangement is intended so as the semiconductor device within an individual dice to withstand the concentrated stress applied at the time of cutting a

semiconductor wafer into a plurality of dices and at the time of mounting a semiconductor device in order to minimize damage due to the applied stress and thereby obtaining high reliability and manufacturing yield rate, see page 6, lines 16-25 of Applicants' original disclosure.

Specifically, independent claim 1 expressly defines a semiconductor device comprising:

"semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion, wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have **means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line** and **exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line.**"

Likewise, independent claim 5 defines a semiconductor device comprising:

"semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a semiconductor element protective layer installed on said semiconductor elements, a stress cushioning layer installed on said semiconductor element protective layer, a first opening formed in said semiconductor element protective layer on said electrode pad, a second opening formed in said stress cushioning layer on said electrode pad, a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad, external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and a conductor protective layer installed on said stress

cushioning layer excluding said external electrodes arranged on said lead wire portion, wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have **means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line** and **exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line**."

Similarly, independent claim 33, as renumbered, defines a semiconductor device comprising:

"at least one semiconductor element including an electrode pad formed on one side along a cutting scribe line;

a stress cushioning layer formed on said semiconductor element;

a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad;

external electrodes installed on said lead wire portion on top of said stress cushioning layer; and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes include **means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line** and **exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line**."

As expressly defined in each of Applicants' independent claims 1, 5 and 33, one of key features is that the stress cushioning layer, the lead wire portion, the conductor protective layer, and the external electrodes include "**means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line** and **exposing a range from said end face on said end surface of said s miconductor elements to an inside of said cutting scribe**

line". In other words, each end face of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), is formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line.

This is necessary so that when a semiconductor wafer is to be cut along the cutting scribe line, the semiconductor wafer can be cut without any damage to semiconductor devices within the cutting scribe line due to application of mechanical stress and thermal stress in order to enhance reliability of the semiconductor devices and increase the production yield rate of the semiconductor devices. See pages 9-10 of Applicants' substitute specification.

In contrast to Applicants' independent claims 1, 5 and 33, Yamamoto '865 discloses none of these features, as expressly acknowledged in the background of Applicants' original disclosure.

Nevertheless, in support of the rejection of Applicants' claims 1, 5 and 33, the Examiner simply asserts that Yamamoto '865 teaches,

> "a semiconductor device (see entire disclosure) comprising an electrode pad (13), a stress cushioning layer 917), a lead wire (14), external electrodes (11), and a conductor protective layer (10) (see Figs. 1-2)."

Notwithstanding the fact that the Examiner has ignored all the essential features of Applicants' independent claims 1, 5 and 33, Yamamoto '865, as

discussed previously, addresses a different problem and the solution disclosed by Yamamoto '865 has problems which are the reasons for Applicants' disclosed invention.

Specifically, Yamamoto '865 proposes to prevent a semiconductor element with a small number of pins such as a memory, a general-purpose microcomputer, etc., from becoming expensive and the miniaturization rate of QFP from becoming small, even if it is made into CSP (chip size package). See Abstract.

For this purpose, the metallic wiring 14 drawn out of the element electrode 13 of a semiconductor element 12 is made on a first resin layer 15, as shown in FIG.2, and the element electrode 13 of the semiconductor element 12 and a package electrode 11 are electrically connected with each other through the metallic wiring 14. Then, the electric connection with outside is performed at the package electrode 11 positioned in the opening of a second resin layer 10. Moreover, the stress cause by the difference of thermal expansion between a mounting board and the silicon (Si) of the semiconductor element 12 when this semiconductor device and an outside mounting board are mounted is relieved by the polyimide resin layer 17, a first resin layer 15, and a second resin layer 10 made on a passivation film 16. Thus, the chip size package (CSP) can be manufactured at lowcost, because they are processed en block in wafer units without performing individual assembly.

While some elements of Yamamoto '865 may be considered as similar to some of Applicants' elements as defined in independent claims 1, 5 and 33, the configuration, arrangement and functions of Yamamoto '865 and Applicants' claimed invention are completely different.

For example, and for the Examiner's convenience, the element electrode 13, as shown in FIG. 2 of Yamamoto '865, may correspond to the electrode pad of Applicants' claimed invention. Similarly, the polyimide resin layer 17, as shown in FIG. 2 of Yamamoto '865, may correspond to the semiconductor protective layer of Applicants' claimed invention. The package electrode 11, as shown in FIG. 2 of Yamamoto '865 may correspond to the external electrode of Applicants' claimed invention. The first resin layer 15, as shown in FIG. 2 of Yamamoto '865, may correspond to the stress cushioning layer of Applicants' claimed invention, and the second resin layer 10, as shown in FIG. 2 of Yamamoto '865, may correspond to the surface protective layer of Applicants' claimed invention.

However, the second resin layer 10, as shown in FIG. 2 of Yamamoto '865, does not correspond to Applicants' claimed "conductor protective layer". Similarly, the polyimide layer 17, as shown in FIG. 2 of Yamamoto '865, does **not** serve as the stress cushioning layer as alleged by the Examiner. Rather, in Yamamoto '865, the stress cushioning layer is the first resin layer 15.

More importantly, in Yamamoto '865, none of the elements is described in anyway to address the damage due to the concentrated stress applied at the time of cutting a semiconductor wafer and at the time of mounting a semiconductor device, see page 6, lines 16-25 of Applicants' original disclosure. As a result, **no** where in Yamamoto '865 is there disclosure or suggestion that all the elements in Applicants' claims 1, 5 and 33 are located inside of the peripheral edge of the semiconductor element.

Nevertheless, in the Advisory Action (Paper No. 17) dated on October 8,

2002, the Examiner asserts that the "polyimide resin layer" of Yamamoto '865 constitutes Applicants' claimed "stress cushioning layer", and more importantly, cites FIG. 13 of Yamamoto '865 for allegedly disclosing:

> "the cutting scribe lines (23) that separate each semiconductor device (24) (consider each square), wherein each semiconductor device include the stress cushioning layer (17), lead wire portion (14), conductive protective layer (10) and external electrodes (11) ... Thus, the stress cushioning layer (17), lead wire portion (14), conductive protective layer (10) and external electrodes (11) of each semiconductor device (24) are **inside the square or cutting scribe lines (23)**, as required by Applicant."

However, the Examiner's assertion as formulated in the Advisory Action (Paper No. 17) is incomplete and misplaced. This is because not only the Examiner has ignored the key limitation of Applicants' independent claims 1, 5 and 33, that is, "means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line", but also misinterpreted the elements inside the cutting scribe line. While it is correct to assert that the semiconductor devices of each individual dice are inside the square or cutting scribe line, there is **no** basis for asserting that the semiconductor layers (forming semiconductor devices across the wafer), for example, the stress cushioning layer and the conductor protective layer, are inside the cutting scribe line.

Typically, all these semiconductor layers are formed across the entire wafer. This is what is shown in FIG. 13 of Yamamoto '865. Specifically, FIG. 13 of Yamamoto '865 shows that all semiconductor devices are within the square or cutting scribe lines. However, all the semiconductor layers constituting those

semiconductor devices are still formed across the entire wafer (18). As shown in FIGs. 2-11 and FIGs. 16-22 of Yamamoto '865, all the semiconductor layers, including, for example, the polyimide resin layer and other resin layers, are formed across the wafer. Only after the resin layers are formed, will the wafer be cut into individual dices. The problem with the approach as disclosed by Yamamoto '865 is that, when the wafer is cut, a large mechanical/temperature stress is applied to the interfaces of the resin layers which, in turn, cause one or more resin layers to peel off and damage the semiconductor devices within each dice. See pages 5-6 of Applicants' original disclosure.

In the interest of expedition, Applicants' independent claims 1, 5 and 33 have been amended to further characterize that **all layers are located inside a peripheral edge of the semiconductor element(s)** as shown in FIG. 1-33 of Applicants' disclosure. For example, independent claim 1 has been amended to further define "such that [the] stress cushioning layer, [the] lead wire portion, [the] conductor protective layer, and [the] external electrodes are located inside of a peripheral edge of said semiconductor elements". Likewise, independent claim 5 has been amended to further define "such that [the] semiconductor element protective layer, [the] stress cushioning layer, [the] lead wire portion, [the] conductor protective layer, and [the] external electrodes are located inside of a peripheral edge of said semiconductor elements." Alternatively, independent claim 33 has been amended to further define "wherein each end face of said stress cushioning layer, and said conductor protective layer is formed on an end surface of said semiconductor element so as to be positioned inside said cutting scribe line and to

be exposed within a range from said end face on said end surface of said semiconductor element to an inside of said cutting scribe line."

In view of the foregoing explanations, and the proposed amendments to independent claims 1, 5 and 33, Applicants respectfully request that the rejection of base claims 1, 5 and 33 under either 35 U.S.C. §102(b) or 35 U.S.C. §103(a) be withdrawn.

Turning now to dependent claims 2, 6, and 34, the Examiner asserts that Yamamoto '865 teaches the end face of the conductor protective layer (10) is formed inside the end face the stress cushioning layer (17). Similarly, regarding dependent claims 3. 7, 8 and 36, the Examiner asserts that Yamamoto '865 teaches the end face of the conductor protective layer (10) is formed outside said end face the stress cushioning layer (17). However, no where in Yamamoto '854 is there a disclosure or suggestion as to how the conductor protective layer is formed on both of inside and outside of the stress cushioning layer. In fact, Applicants cannot understand as to how the conductor protective layer can be formed on both inside and outside of the stress cushioning layer as alleged by the Examiner.

As can be seen from FIG. 2, elements 11 and 12 of Yamamoto '865, the elements have the peripheral edges located the peripheral edge of the semiconductor element. As a result, the element construction of Yamamoto '865 is completely different from the element construction of Applicants' claims 1, 5 and 33.

In summary, Applicants respectfully submit that Yamamoto '865 fails to disclose or suggest virtually all the essential features of Applicants' claims 1-10 and 28-36. As a result, Applicants respectfully request that the rejection of claims 1-10

and 28-36 under either under 35 U.S.C. §102(b) or under 35 U.S.C. §103(a) be withdrawn.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

In view of the foregoing amendments, arguments and remarks, all claims 1-10 and 28-36 are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

Please charge any shortage in the fees due in connection with the filing of this paper, to Deposit Account No. 01-2135, and please credit any excess fees to such deposit account.

Respectfully submitted,
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